Claims

What is claimed is:

[c1] A computer system comprising:

a processor;

an object cache operatively connected to the processor;

a memory; and

a translator interposed between the object cache and the memory, wherein the translator maps an object address to a physical address within the memory.

[c2] The computer system of claim 1, wherein the object address comprises an object identification number and an offset.

[c3] The computer system of claim 1, wherein the object address is encoded by the processor using an extended address encoding procedure.

[c4] The computer system of claim 3, wherein the extended address encoding procedure embeds the object address into an unused part of a physical address range.

[c5] The computer system of claim 1, wherein the translator maps the object address to the physical address using a table.

[c6] The computer system of claim 1, wherein the processor uses an extended instruction set.

[c7] The computer system of claim 1, wherein the translator converts operations using the object address into operations using the physical address.

[c8] The computer system of claim 1, wherein the translator loads a plurality of cache lines from the memory.

[c9] The computer system of claim 1, wherein the translator allocates physical memory a first time a portion of an object is evicted from the object cache.

[c10] A computer system comprising:

a plurality of processors;

an object cache operatively connected to the plurality of processors;

a memory; and

a translator interposed between the object cache and the memory, wherein the translator maps an object address to a physical address within the memory.

[c11] The computer system of claim 10, wherein the object address comprises an object identification number and an offset.

[c12] The computer system of claim 10, wherein the object address is encoded by one of the plurality of processors using an extended address encoding procedure.

[c13] The computer system of claim 12, wherein the extended address encoding procedure embeds the object address into an unused part of a physical address range.

[c14] The computer system of claim 10, wherein the translator maps the object address to the physical address using a table.

[c15] The computer system of claim 10, wherein the plurality of processors uses an extended instruction set.

[c16] The computer system of claim 10, wherein the translator converts operations using the object address to operations using the physical address.

[c17] The computer system of claim 10, wherein the translator loads a plurality of cache lines from the memory.

[c18] The computer system of claim 10, wherein the translator allocates physical memory a first time a portion of an object is evicted from the object cache.

[c19] A method for retrieving an object in a single processor environment comprising:
obtaining an object address corresponding to the object;
determining if the object address corresponds to a tag in a tag array of a cache;
retrieving the object address if the tag corresponding to the object address is in the tag array;
translating the object address into a physical address if the object address is not in the tag array; and
retrieving a cache line using the physical address if the object address is not in the tag array.

[c20] The method of claim 19, further comprising:
entering the cache line into the cache.

[c21] The method of claim 19, wherein the object address comprises an object identification number and an offset.

[c22] The method of claim 21, wherein a word within the object is retrieved using the offset.

[c23] The method of claim 19, wherein the object address is encoded using an extended address encoding procedure.

[c24] The method of claim 23, wherein the extended address encoding procedure embeds the object address into an unused part of a physical address range.

[c25] The method of claim 19, wherein the step of translating the object address uses a translator.

[c26] The method of claim 25, wherein the translator converts operations using the object address to operations using the physical address.

[c27] The method of claim 25, wherein the translator loads a plurality of cache lines from the memory.

[c28] A method for retrieving an object in a multiprocessor environment comprising:
obtaining an object address corresponding to the object;
determining if the object address corresponds to a tag in a tag array of a cache;
retrieving the object if the tag corresponding to the object address is in the tag array;
translating the object address into a physical address if the object address is not in the tag array; and
retrieving the object using the physical address if the object address is not in the tag array.

[c29] The method of claim 28, further comprising:
entering the cache line into the cache.

[c30] The method of claim 28, wherein the object address comprises an object identification number and an offset.

[c31] The method of claim 30, wherein a word within the object is retrieved using the offset.

[c32] The method of claim 28, wherein the object address is encoded using an extended address encoding procedure.

[c33] The method of claim 32, wherein the extended address encoding procedure embeds the object address into an unused part of a physical address range.

[c34] The method of claim 28, wherein the step of translating an object address uses a translator.

[c35] The method of claim 34, wherein the translator converts operations using the object address to operations using the physical address.

[c36] The method of claim 34, wherein the translator loads a plurality of cache lines from the memory.